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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,762	10/15/2003	Shiv Kumar Gupta	15164US01	6313

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EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

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03/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,762	GUPTA, SHIV KUMAR	
	Examiner	Art Unit	
	KIBROM K. GEBRESILASSIE	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003 and 21 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/07/2008 has been entered.

2. Claims 1-11 are presented for examination.

3. Claims 6-11 have been canceled previously.

Response to Arguments

4. Applicant's arguments, filed on 01/07/2008, have been fully considered and are persuasive.

5. Applicant's arguments relating to 101 rejection are persuasive and the rejection is withdrawn. However, note a new 101 rejection.

6. Applicant's arguments relating to art rejection are persuasive but are moot in view of the new ground(s) of rejection.

Drawings

7. New corrected drawings in compliance with 37 CFR 1.121(d) is required in this application because the drawings are illegible (See, for example Figs. 4 and 5).

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid

abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-5 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims are directed to a judicial exception to 35 U.S.C. 101 (**i.e., a abstract idea,** natural phenomenon, or law of nature) and is not directed to a practical application of such judicial exception because the claim does not require any physical transformation and the invention as claimed does not produce a useful, concrete, and tangible result.

For example, the claimed subject matter does not produce a useful or tangible result:

a. A **useful** result is missing because the claim subject matter fails to identify a specific and substantial result, for example, the claimed invention related to "verifying the system". However, the claimed invention is used for verifying ***unspecified*** condition of a system.

> a) "USEFUL RESULT"
>
> For an invention to be "useful" it must satisfy the utility requirement of section 101. The USPTO's official interpretation of the utility requirement provides that the utility of an invention has to be (i) specific, (ii) substantial and (iii) credible. MPEP § 2107 and *Fisher*, 421 F.3d at 1372, 76 USPQ2d at 1230 (citing the Utility Guidelines with approval for interpretation of "specific" and "substantial"). In addition, when the examiner has reason to believe that the claim is not for a practical application that produces a useful result, the claim should be rejected, thus requiring the applicant to distinguish the claim from the three 35 U.S.C. 101 judicial exceptions to patentable subject matter by specifically reciting in the claim the practical application. In such cases, statements in the specification describing a practical application may not be sufficient to satisfy the requirements for section 101 with respect to the claimed invention. Likewise, a claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of a section 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected.

b. A **tangible** result is missing because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or a manipulation data. More specifically, the claims subject matter provides a "testing result". However, there is no link between the "testing result" and the rest of the steps. This produced result remains in the abstract, and, thus, fails to achieve the required status of having real world value.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For example,

a. Claims 1, and 4, the claims recite “providing a testing results”, but it is unclear which “testing result" referring to.

b. Claims 1, and 4, the claims recite "first circuitry further **comprising** at least one **output**". It is unclear what applicants mean by "output". Is it part of the "circuitry" or "result"?

c. Claim 1 recites:

> **a hardware emulator for verifying** the plurality of systems on the plurality of chips, said hardware emulator further comprising:
> **a first circuitry for verifying** a first system on a chip, said first circuitry further comprising at least one output for providing testing results from the first system on the chip; and
> **a second circuitry for verifying** a second system on another chip while verifying the first system on chip.

i. There is no any link between each steps.

ii. The claim is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the “connection” between the first circuitry and second circuitry.

Applicants Admission

11. Applicant’s disclosure states as follows:

Prior art:

[0006] Many chip-makers now use a device called a hardware emulator to verify SOCs. A hardware emulator is a device with large amounts of logic and other circuitry with highly configurable connections. The connections can be configured so as to realize the design of the SOC. The design is usually described in a data structure. A script checks the capacity of the hardware emulator to determine whether the hardware emulator has sufficient logic and circuitry to realize the design described in the data structure. If the hardware emulator has sufficient capacity to realize the design described in the data structure, the script places the data structure in a top wrapper. The top wrapper parses the data structure describing the design and configures the hardware emulator to realize the design.

Compare to claimed invention:

[0023] **FIGURE 2** is a block diagram of a hardware emulator configured in accordance with an embodiment of the present invention. The hardware emulator 200 comprises a sea of logic and other circuitry 205. The sea of logic and other circuitry 205 is configurable to realize a vast number of integrated circuits. The sea of logic and other circuitry can be divided into a plurality of portions 210,

[0026] The emulator 200 of FIGURE 2 can be configured by a computer system configured generally as described in FIGURE 3. An SOCs, SOC1...SOCn can be described in a data structure in a file. The file is parsed by a script. A script is a plurality of executable instructions stored in the memory of the computer system, or a removable memory, that parses the data structures, checks the capacity of the emulator 200, and creates another file, known as a top wrapper. The top wrapper is provided to the emulator and configures the emulator 200 in accordance with the SOCs described in the data structure.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(f) he did not himself invent the subject matter sought to be patented.

13. Claims 1-5 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter.

Comment [K1]: Its okay, however, it is after the 1st round of prosecution and specially rejected using peiece of prior art. I would like to also see additional prior art rejection on record as well.

a. Applicant's admission establishes that applicant has invented a system of using a hardware emulator for verifying a plurality of systems of the prior art. Applicants have not disclosed inventing a hardware emulator system. As such, any claims directed to a system that facilities this system must be regarded as being invented by another.

a. These rejection may be overcome by evidence that applicant has somehow transformed the hardware emulator system of the prior art by some specialization. As currently disclosed, however, applicants' system of verifying using a hardware emulator merely uses the existing feature of the prior art.

b. Evidence that hardware emulator anticipates the invention of claims 1-5 is found in applicant's admission as explicitly recited in the disclosure of the invention.

14. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by US Publication No. 2004/0019827 issued to Rohfleisch et al.

As per claim 1:

Rohfleisch discloses a system for verifying a plurality of systems on a plurality of chips (**See: [0001]**), said system comprising:

a hardware emulator (**See: Fig. 1 #110 and corresponding texts**) for verifying the plurality of systems on the plurality of chips (such as *processor core 102, and other core 106 of Fig. 1*), said hardware emulator further comprising:

a first circuitry for verifying a first system on a chip (**See: Fig. 1 #104 and corresponding texts**), said first circuitry further comprising at least one output for providing testing results from the first system on the chip (**See: Fig. 1 # 112, #114 and corresponding texts**); and

a second circuitry for verifying a second system on another chip while verifying the first system on chip (**See: Fig. 1 # 108 and corresponding texts**).

As per claim 2:

Rohfleisch discloses the system of claim 1, wherein the hardware emulator further comprises:

a first interface for providing inputs to the first circuitry and receiving outputs from the first circuitry (**See: Fig. 1 # 112, #114 and corresponding texts**); and

a second interface for providing inputs to the second circuitry and receiving outputs from the second circuitry (**See: Fig. 1 # 116, #118 and corresponding texts**).

As per claim 3:

Rohfleisch discloses the system of claim 1, wherein the first circuitry is configured to realize the first system on a chip and the second circuitry is configured to realize the second system on another chip (**See: Fig. 1 #104, #108 and corresponding texts)**.

As per claim 4:

Rohfleisch discloses a system for verifying a plurality of systems on a plurality of chips (**See: [0001]**), said system comprising:

a hardware emulator (**See: Fig. 1 #110 and corresponding texts**) comprising:

a first circuitry configured to realize a first system on a chip (**See: Fig. 1 #104 and corresponding texts**), said first circuitry further comprising at least one output for providing testing results from the first system on the chip (); and

a second circuitry configured to realize a second system on another chip while verifying the first system on chip, the second circuitry connected to the first circuitry (**See: Fig. 1 # 108 and corresponding texts**).

As per claim 5:

Rohfleisch discloses the system of claim 4, wherein the hardware emulator further comprises:

a first interface operably connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry (**See: Fig. 1 # 112, #114 and corresponding texts**); and

a second interface operably connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry (**See: Fig. 1 # 116, #118 and corresponding texts**).

As per claim 6-11. (Cancelled).

Conclusion

15. All claims are rejected.

16. The prior art made of record on PTO-892 and not relied upon is considered pertinent to applicant's disclosure.

Examiner Remarks

17. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. **Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and**

figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Examiner Request

18. **In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on** for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

MPEP states:

"…with respect to newly added or amended claims, applicant should show support in the original disclosure for the new or amended claims. See MPEP § 714.02 and § 2163.06."

Communications

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is 571-272-8571. The examiner can normally be reached on 8:00 am - 4:30 pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. K. G./
Examiner, Art Unit 2128

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128